ABSTRACT

A method of fabricating nitride read-only memory (NROM) cells and arrays. The memory device is formed on a substrate. Each memory cell comprises a pair of bit lines extending in a first direction across the substrate, a pair of bit line dielectrics overlaying and covering the pair of bit lines, a charge-trapping layer formed over the channel region between the pair of bit lines, and a conductive connecting block formed on the charge-trapping layer. The charge-trapping layer comprising two oxide-nitride-oxide (ONO) structures separated by a gate oxide layer, where each ONO structures comprises a layer of nitride sandwiched between a bottom oxide layer and a top oxide layer. A plurality of straight, parallel-edged word lines extend across the substrate in a second direction and cross over the bit lines and channel regions. Each word line comprises a conductive material and is separated from the substrate by the conductive connecting blocks and bit lines dielectrics.